NAGASE

July 21, 2011

Nagase & Co., Ltd.

Nagase Strengthens Semiconductor Materials Business

—New Organization to Focus on Materials and Mounting Technology—

Tokyo, Japan, July, 21, 2011—Nagase & Co., Ltd. (Tokyo, Japan; TSE: 8012) announces that it has formed a new organization, the Semiconductor Materials Division, under the Electronic Chemicals Department to strengthen the semiconductor materials business by bringing together into one group various materials for front-end and back-end processing along with the processing business.

- About the Semiconductor Business -

The Nagase Group has supplied the semiconductor market with various products and solutions developed and manufactured by Nagase ChemteX (Osaka, Japan; President: Mitsukuni Mori), a wholly owned subsidiary. At its Harima site, Nagase ChemteX has also begun a wafer bumping* service as part of its back-end semiconductor processing business in response to growing market interest in micron mounting. The company will focus on solder bump processing as it expands its micron bump bonding business amid widening adoption by the electronics industry.

*Wafer bumping: Bumps are formed on each wafer when attaching a bare chip to a mounting substrate.

- About the Micro Bump Business -

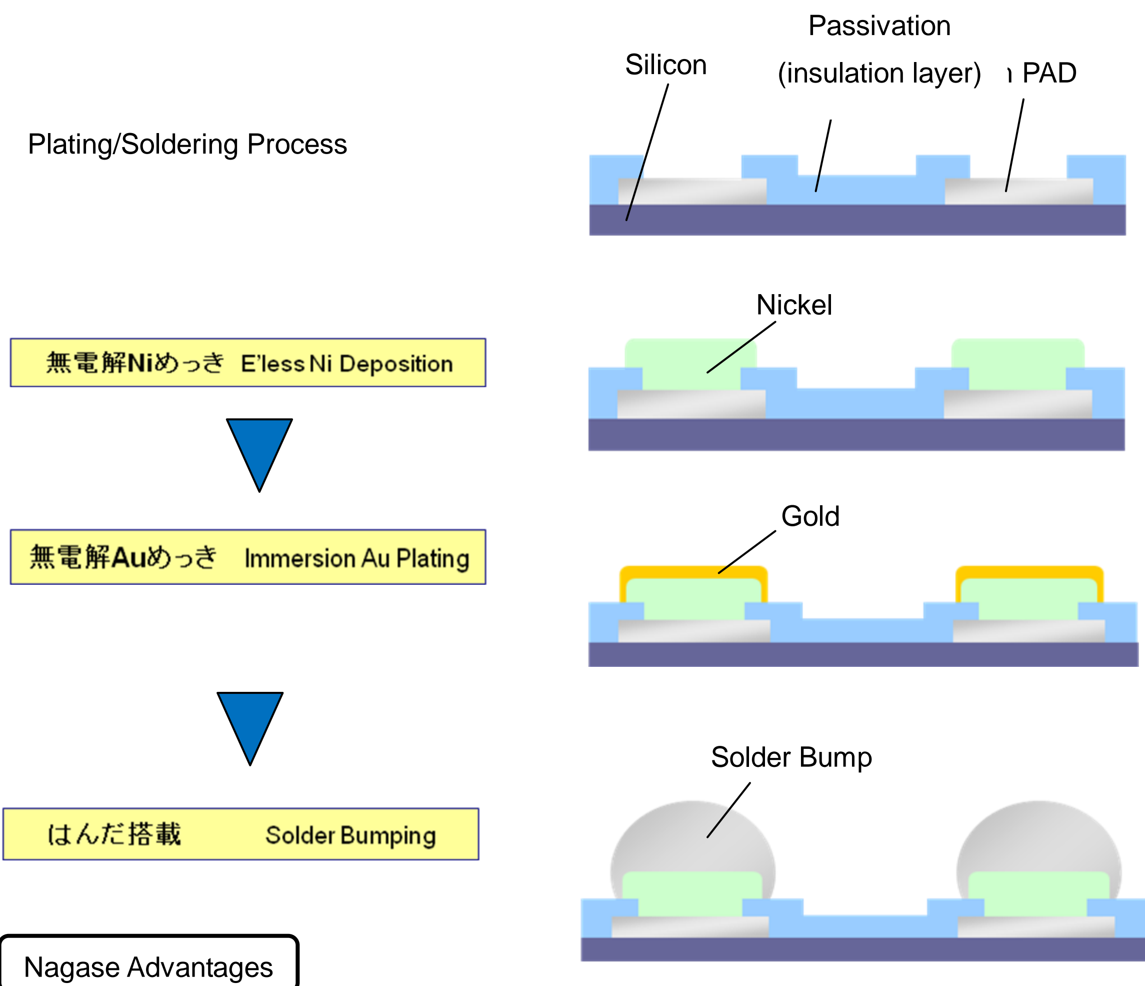
Nagase Group company Pac Tech-Packaging Technologies Gmbh (Nauen, Germany; CEO: Elke Zakel) became the first in the world to engineer for mass production a maskless process for plating the semiconductor wafer's pad electrode which uses the Under Bump Metallization (UBM) techniques of electroless Ni deposition and immersion Au plating. The development of the process has solidified the company's position as a market leader in wafer processing. Our micro bumping technology provides 60um solder ball mounting for 4～12 inch wafers. The process is available for various types of wafer (Si, Backside Metalized Si compound semiconductors), and mass production of wafers for mobile electronics applications has already begun.

The Nagase Advanced Assembly Development Center is leading the Group's development of 3D Assembling Technology with micro solder bumps In the future, the Nagase Group plans to offer Assembly technology and mounting materials (sealants), including solder bumping technology for 50um pitch and lower, for which demand is expected to grow.

In the semiconductor materials business, Nagase has long served customers with liquid semiconductor encapsulation (LSE) products, resist products, and stripping agents. In 2010, the product lineup was bolstered through the conclusion of a chemical solution manufacturing license with Alchimer S.A. of France (Massy, France; CEO: Mr. Steve Lerner). Under the deal, Nagase will strive towards the early commercialization of fill technology and materials (all-wet process, chemical solutions) for through-silicon vias (TSV). The strong synergies generated by the deal will support the development of three-dimensional mounting technology with the aim of offering total solutions to help raise the presence and value of Nagase and expand sales. We hope to expand the global semiconductor business to ¥6.0 billion in fiscal 2011 and to ¥10.0 billion in a few years time.

Nagase will continue to build a unified business structure within the Group and expand its semiconductor business through the generation of strong synergies.

(Reference Material)



- ●Fast delivery using maskless, continuously automatic electroless UBM process
- ●Applicable for various wafers: silicon, Backside Metalized Si, compound semiconductors
- ●Chip, applicable for 2 to12 inch wafers
- ●FC micron solder bump (100um pitch), WLP solder bump (300um pitch)
- ●UBM ideal for Au and Cu wire bonding substrate
- ●Liquid semiconductor encapsulants for FC, WLP also available

Overview of Nagase & Co., Ltd.

Established	December 9, 1917
Head Office	5-1, Nihonbashi-Kobunacho, Chuo-ku, Tokyo
Paid-in Capital	9,699 million yen
Main Business	Import/export and domestic sales of chemicals, plastics, electronics materials, cosmetics and health foods
URL	http://www.nagase.co.jp/english/

Inquiries about this announcement:

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Wafer Bumping Section

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